

REMARKS

I. STATUS OF CLAIMS

Claims 1-23 are currently pending. Claims 15-23 have been allowed. Claims 2, 3, 4, 5, 7, 9, and 11 were objected to due to various informalities. Claims 2, 3, 4, 5, 9, 11, and 18 were amended.

II. REJECTIONS UNDER 35 U.S.C. § 103

In item 5 on page 3 of the Office Action, claims 1, 2, 4-7, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,721,546 (Tsutsumishita) in view of U.S. Patent No. 5,400,148 (Kashida).

Applicants respectfully submit that independent claim 1, for example, is patentable over the references, as neither Tsutsumishita nor Kashida, alone or in combination, teaches or suggests, "delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in a second path that is different from the first path."

In contrast to the present invention, Tsutsumishita discloses A/D converters 8A, 8B, and an arithmetic circuit 9 for converting digital data generated by the A/D converters 8A and 8B into position data. See Tsutsumishita, column 1, lines 37-42.

Kashida discloses supplying to the color-differential signal sequential circuit 24 a timing signal whose passage as been delayed by a time corresponding to the time delay generated by the Audio/Digital converters 18 and 20. Kashida further discloses supplying to the timing control circuit 88 a synchronizing signal produced by delaying the passage of the synchronizing signal by a time corresponding to the time delay generated by the color-differential signal sequential circuit 24 and supplying to the timing control circuit 88 a timing signal produced by delaying passage of the drum rotating signal by a time corresponding to the time required to read out data from the frame memory 22. See Kashida, column 5, lines 8-36. In Kashida, digital signals are delayed (two timing signals and synchronizing signals).

Kashida does not disclose delaying an analog signal. Accordingly, it is not possible to control an analog signal in synchronism with a digital control signal regardless of the process delay caused by analog-digital converting (ADC 14) and arithmetic processing (arithmetic processing circuit 15). By delaying an analog signal, the present invention can control a current analog signal as well as a future analog signal, as an analog signal can be delayed independently of a digital signal. Therefore, claims 1, 6, 7, and 14 (claims 6, 7, and 14 recite

similar language, in relevant part) of the present invention are patentable over the references. As dependent claims 2, 4, and 5 depend from independent claim 1, the dependent claims are patentable over the references for at least the reasons presented for the independent claim.

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsutsumishita in view of U.S. Patent No. 6,563,859 (Oishi). Applicants respectfully submit that although Oishi discloses delay units, Oishi does not add any relevant information to Tsutsumishita. As claim 8 depends from independent claim 7, claim 8 is patentable over the combination, as the combination does not teach or suggest a delay circuit for delaying an analog signal, as recited in claim 7.

Similarly, although Gurvich discloses a group delay adjusting circuit, Gurvich does not add any relevant information to Tsutsumishita. The combination of references does not teach or suggest a delay circuit for delaying an analog signal. Therefore, claims 12 and 13, via independent claim 7, are patentable over the references.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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